EE/CPRE/SE 4920 - sddec24-13

ReRAM Compute ASIC Fabrication

Weekly Report 2

9/6/2024 - 9/19/24

Client: Prof. Henry Duwe

Advisor: Prof. Cheng Wang

Team Members:

- Gage Moorman - Team Organizer, main analog designer
- Konnor Kivimagi - Main documentation editor, mixed analog digital designer
- Nathan Cook – Main client liaison, mixed analog digital designer
- Jason Xie – Assistant documentation editor, main digital designer

Weekly summary:

We are still running into some issues with getting our designs to pass the precheck step but we are working very hard to fix this issue as it is a project killing issue. We also mapped out a plan for the SoC pins and created a plan to test them. We also worked on debugging importing Openlane spice files into Xschem.

Past Week Accomplishments:

- Got very close to pushing the reram cell through the MPW precheck
- SoC pins mapped and documented, process for testing pins has been created.
- Determined Analog VDD and VSS pins and what voltages they will be

Individual Contributions:

Team Member	Contributions	Weekly hours	Total Hours
Konnor Kivimagi	Working on getting reram through precheck	40	106
Gage Moorman	Still working on layout and analysis for adc. Determined analog VDD and VSS	7	73
Nathan Cook	Logic analyzer and GPIO pin configurations documented. Process for c test code in progress	7	71
Jason Xie	Sitll working to import encoder into Magic and Xschem for post-synthesis testing.	7	71

Pending Issues:

- Gate level simulation for digital hardening is having issues

    - Having some issues correctly flattening and importing spice files into Xschem
- Precheck through efabless
- Having difficulty using ngspice and xschem analysis tools effectively

Plans for the coming week:

- Gage Moorman
    - Finish Comparator and ADC layout and Hardening
    - Build upon analog documentation
    - Do ADC matching analysis
- Konnor Kivimagi
    - Finish verifying precheck and parasitics on 1T1R ReRam cell
    - Design and create layouts for larger 4x4 and 8x8 ReRam arrays
- Nathan Cook
    - Write and run logic analyzer test case
    - Create in depth documentation for pins and top-level design including pin locations
- Jason Xie
    - Troubleshoot issues importing spice file generated by Openlane into Xschem
    - Assist in writing C test code for control and GPIO

Summary of Advisor Meeting:

During our meetings, we went over some of the finer details of our design, such as how each of the individual components were going to connect as well as how we would provide power reliably to the device. Another topic was that we should prioritize getting something fabricated over getting the whole circuit working as the more that we could get back from the fab the better.